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| EXAMINER | |
|---|---|
| KNOLL, CLIFFORD H | |

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| 2112 | |

DATE MAILED: 09/30/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/736,567 | BRENNER ET AL. | |
| | Examiner | Art Unit | |
| | Clifford H Knoll | 2112 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *02 September 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-24, 26-28, 32* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-24, 26-28, 32* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

This Office Action is responsive to communication filed 7/26/2004. Currently claims 1-24, 26-28, and 32 are pending . Claims 25 and 29-31 have been cancelled.

The text of those sections of Title 35, U.S. Code not included in this action can be found in a prior Office action.

### *Claim Rejections - 35 USC § 103*

*Claims 1-24, 26-28, and 32 stand rejected under 35 U.S.C. 103(a) as being unpatentable over Bhagat (US 2002/0016880) in view of standard exception practice in ARM processors, as evidenced by "ARM application note 25: Exception handling on the ARM (including thumb-aware processors)" ("Note 25", hereinafter), further in view of "ARM application note 31: using embeddedICE" ("Note 31", hereinafter).*

Regarding claim 1, Bhagat discloses the interrupt vector table with first and second vector addresses executable, the first vector address preceding the second vector address in the vector table (e.g., paragraph [0027]), providing a common interrupt dispatcher (e.g., paragraph [0043], "common routine"), inserting an instruction into the first vector address that disables the first vector address (e.g., paragraph [0027]), inserting an other instruction that branches to the common interrupt dispatcher, providing the common interrupt dispatcher with

an interrupt routine (e.g., paragraph [0026], "ISR instruction"), and then re-enables the second interrupt modes, wherein requests are processed without interruption (e.g., paragraph [0027], "globally disable").

Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as evidenced by Note 25. Note 25 discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common interrupt handler of Bhagat. Therefore it would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

Regarding claim 2, Bhagat also discloses inserting a single instruction that disables both interrupt modes (paragraph [0027], "globally disable"). Bhagat

does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (e.g., p. 12, "ORR r13, r13, 0xC0").

Regarding claim 3, Bhagat also discloses re-enabling the interrupt modes (e.g., paragraph [0029]).

Regarding claim 4, Bhagat also discloses determining whether a received interrupt was the first or second type (e.g., paragraph [0031]).

Regarding claim 5, Bhagat also discloses checking the mode identifier (e.g., paragraph [0048]).

Regarding claim 6, Bhagat also discloses where an interrupt routine with an instruction branches to the first and second interrupt handlers (e.g., paragraph [0043]).

Regarding claim 7, Bhagat also discloses the IRQ and FIQ interrupt types (e.g., paragraph [0037]).

Regarding claim 8, Bhagat discloses the single instruction (e.g., paragraph [0027], "globally disable"). Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (e.g., p. 12, "ORR r13, r13, 0xC0").

Regarding claim 9, Bhagat discloses providing a common interrupt handler (e.g., paragraph [0043]), inserting into an IRQ vector address of an interrupt vector table, an instruction that disables an FIQ interrupt mode (e.g., paragraph [0028], "global disable may be enforced"), inserting at the FIQ vector address an instruction that branches to the common interrupt dispatcher (e.g., paragraph [0043]), providing the common interrupt dispatcher with an interrupt

routine that processes an interrupt and the re-enables the FIQ interrupt mode (e.g., paragraph [0029]), processing interrupts without interruption (e.g., paragraph [0029]).

Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as evidenced by Note 25. Note 25 discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common interrupt handler of Bhagat. Therefore it would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

Regarding claim 10, Bhagat also discloses inserting a single instruction that disables both interrupt modes (paragraph [0027], "globally disable"). Bhagat

does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (e.g., p. 12, "ORR r13, r13, 0xC0").

Regarding claim 11, Bhagat also discloses re-enabling the interrupt modes (e.g., paragraph [0029]).

Regarding claim 12, Bhagat also discloses determining whether a received interrupt was an IRQ or an FIQ interrupt (e.g., Figure 2, "204", "206").

Regarding claim 13, Bhagat also discloses checking the mode identifier (e.g., paragraph [0031]).

Regarding claim 14, Bhagat also discloses where an interrupt routine with an instruction branches to the FIQ and IRQ interrupt handlers (e.g., paragraph [0043]; Figure 3, "310", "318").

Regarding claim 15, Bhagat discloses providing a common interrupt handler that checks a mode identifier to determine whether of first or second type (e.g., Figure 2, "204", "206"), inserting and executing another instruction that branches to the common interrupt handler (e.g., paragraph [0027]), branching to the first vector address, receiving an interrupt of the first type and setting the mode identifier to indicate an interrupt of the first type was received (e.g., Figure 3, "302"), inserting into a first vector address an instruction that disables subsequent interrupts of the first and second type (e.g., paragraph [0029]), executing an instruction to disable first and second type interrupts (e.g., paragraph [0029]), processing the interrupt of the first type with the common interrupt dispatcher without interruptions and re-enabling first and second types (e.g., paragraph [0029]).

Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as evidenced by Note 25. Note 25 discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common interrupt handler of Bhagat. Therefore it would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

Regarding claim 16, Bhagat also discloses first and second types as IRQ and FIQ (e.g., Figure 2).

Regarding claim 17, Bhagat discloses providing a common interrupt handler that checks a mode identifier to determine whether of first or second type (e.g., Figure 2, "204", "206"), inserting at the second vector address and

branching and executing another instruction that branches to the common interrupt handler (e.g., paragraph [0027]).

Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as evidenced by Note 25. Note 25 discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common interrupt handler of Bhagat. Therefore it would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

Regarding claim 18, Bhagat also discloses first and second types as IRQ and FIQ (e.g., Figure 2).

Regarding claim 19, Bhagat discloses an instruction that disables first and second interrupt types, disposed in a first vector address of an interrupt vector table executable upon receipt of an interrupt of the first type (e.g., paragraph [0029]), an other instruction at the second address that branches to a common interrupt handler (e.g., paragraph [0027]), a common interrupt handler that checks a mode identifier to determine whether of first or second type (e.g., Figure 2, "204", "206"), processes the interrupt and re-enables the first and second interrupt types (e.g., paragraph [0029]). Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common interrupt handler of Bhagat. Therefore it would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

Regarding claim 20, Bhagat also discloses processing the interrupts without interruption (e.g., paragraph [0029]).

Regarding claim 21, Bhagat also discloses first and second types as IRQ and FIQ (e.g., Figure 2).

Regarding claim 22, Bhagat discloses providing the claim 21 system (e.g., Figure 2), executing a single instruction to disable IRQ and FIQ interrupts and re-enabling IRQ and FIQ interrupts (e.g., paragraph [0029]), executing an instruction to branch to the common interrupt handler (e.g., paragraph [0027]) and processing the IRQ without interruption (e.g., paragraph [0029]) executing a

single instruction receiving an IRQ interrupt, setting the mode identifier, and branching to an IRQ vector address (e.g., Figure 3, "302").

Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as evidenced by the ARM Application Note. The Note discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common interrupt handler of Bhagat. Therefore it would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

Regarding claim 23, Bhagat discloses providing the system of claim 21 (e.g., Figure 2), receiving an FIQ interrupt, setting the mode identifier and executing the instruction at the FIQ vector to branch to the common interrupt

dispatcher (e.g., Figure 2), and processing the FIQ interrupt without interruption (e.g., paragraph [0029]).

Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as evidenced by Note 25. Note 25 discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common interrupt handler of Bhagat. Therefore it would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

Regarding claim 24, Bhagat discloses an instruction that disables first and second interrupt types (e.g., paragraph [0029]), an instruction that branches to a common interrupt dispatcher (e.g., paragraph [0027]), a common interrupt

dispatcher that checks a mode identifier to determine whether a received interrupt was of the first or second type and processes the interrupt (e.g., paragraph [0027]).

Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as evidenced by Note 25. Note 25 discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common interrupt handler of Bhagat. Therefore it would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

Regarding claim 26, Bhagat discloses code for a dispatcher for a processor with first and second interrupt modes, with the second higher than the

first and interrupt vector table with first and second vector addresses (e.g., paragraph [0030]), a mode status indicator (e.g., Figure 3, "302"), code for inserting an instruction into the first vector address that disables first and second interrupts (e.g., paragraph [0029]), code for inserting an instruction that branches to a common interrupt dispatcher (e.g., paragraph [0027]), and code for providing the dispatcher with an interrupt routine that checks the mode identifier to determine which type (e.g., paragraph [0027]).

Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however this is a standard practice in ARM interrupt processing as evidenced by the ARM Application Note. The Note discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor. Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common interrupt handler of Bhagat. Therefore it

would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

Regarding claim 27, Bhagat also discloses branches first and second interrupts to first and second handlers (e.g., Figure 3, "318", "314").

Regarding claim 28, Bhagat also discloses IRQ and FIQ (e.g., Figure 2).

Regarding claim 32, Bhagat discloses providing a processor with first and second interrupt modes to accept interrupt requests of first and second types (e.g., Figure 2, "IRQ", "FIQ"), a mode status indicator (e.g., Figure 3, "302"), code for inserting an instruction into the first vector address that disables the first and second interrupts (e.g., paragraph [0029]), a processor to execute the instruction in the interrupt table without interruption (e.g., paragraph [0023]), providing a common interrupt dispatcher (e.g., paragraph [0027]), inserting an instruction that disables the second interrupt mode (e.g., paragraph [0029]), providing the common interrupt dispatcher with an interrupt routine that processes the interrupt and re-enables the second interrupt modes (e.g., paragraph [0029]).

Bhagat also discloses a global enable (e.g., paragraph [0029]), but fails to expressly mention its use subsequent to processing the interrupt; however Examiner takes Official Notice that this is a standard practice in ARM interrupt processing as evidenced by Note 25. Note 25 discloses that interrupts are disabled and only enabled after interrupt processing (e.g., p. 22). It would be obvious to combine the Note with Bhagat because the Note discloses standard practical details of exception handling in an ARM processor which are advantageously adhered to when exception handling in an ARM processor.

Therefore it would be obvious to one of ordinary skill in the art to combine Bhagat with standard practice of ARM exception handling to obtain the claimed invention.

Bhagat does not expressly mention a single instruction by itself accomplishing this; however, this is disclosed by Note 31 (pp. 11-12). It would be obvious to combine Note 31 with Bhagat because Note 31 teaches specific instruction details in the vector table that allow common interrupt handling in an ARM processor, such as the common interrupt handler of Bhagat. Therefore it would be obvious to one of ordinary skill in the art to combine Note 31 with Bhagat to obtain the claimed invention.

***Response to Arguments***

Applicant's arguments filed 7/26/04 have been fully considered but they are not persuasive.

Rejections using Bhagat, and using Bhagat in view of widely used exception practice have been withdrawn, in response to amendatory language. However the rejection supra has been maintained.

Regarding claims 1, 9, 15, 17, 19, 22-24, 26 and 32, Applicant argues that Bhagat appears to disclose interrupt merging, but it "does not do so at the chip or processor level". Examiner agrees; however, in the rejection maintained supra, Examiner relies on Note 31 for this feature.

Regarding the use of Note 31 (full citation supra), Applicant argues that Note 31 "is not intended to be an example of how to initialize vectors from a running program. It also does not attempt to describe a process for merging interrupt streams received from IRQ and FIQ devices at IRQ and FIQ vectors" (p. 23); however, Examiner relies not on Note 31, but rather on Bhagat for this feature.

Applicant argues in the sequel that "[t]his Note [31] includes an exemplary code fragment that places an interrupt handler at the FIQ vector address (0x1C). This example uses a Move to Status Register instruction to disable interrupts. However, this instruction is placed at the FIQ vector address rather than at the IRQ vector address as taught by Applicants. Instead, the example places a No-Operation (NOP) instruction at the IRQ address (0x18).... Although the NOP may inherently allow an IRQ exception to fall through to the FIQ address, it would do so without ensuring that the FIQ interrupt is disabled first" (p. 24). Examiner concurs; however, Examiner relies on Note 31 specifically to teach the use of a disable command, which instruction at 0x1C indisputably is, in place of the conventional branch, and to allow the processing to fall through to the next contiguous instruction. Although it is conventional to place a branch at the vector table address, it is a common alternative practice in assembly coding to use fall through instructions in vector tables. Note 31 teaches precisely this practice (used at both the IRQ and FIQ vector addresses 0x18 and 0x1C), and is thus relied upon in the above rejection to teach the fall through technique, as well as to teach the particular use of the disable interrupt command as the fall through

command. These implementation details taught by Note 31 are deemed appropriately combined with the general disclosure of Bhagat in the rejection supra.

Thus the rejection of claims 1-32 is maintained.

## *Conclusion*

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Clifford H Knoll whose telephone number is 703-305-8656. The examiner can normally be reached on M-F 0630-1500.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mark H Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

chk

Khanh Dang
Primary Examiner